



CIRCUIT BREAKER 3VA1 IEC FRAME 160 BREAKING CAPACITY
CLASS S ICU=36KA @ 415 V 2-POLE, LINE PROTECTION
TM210, FTFM, IN=50A OVERLOAD PROTECTION IR=50A FIXED
SHORT CIRCUIT PROTECTION II=10 X IN CABLE CONNECTION

Model	
Product brand name	SETRON
Product designation	Molded case circuit breaker
Design of the product	Line protection
Design of the overcurrent release	TM210
Protective function of the overcurrent release	LI
Number of poles	2
General technical data	
Tension assignée d'isolement Ui	500 V
Max. rated operational voltage Ue with AC 50/60Hz	415 V
Max. rated operational voltage Ue with DC	250 V
Active power loss / for rated value of the current / at AC / in hot operating state / per device	9.7 W
Active power loss / for rated value of the current / at AC / in hot operating state / per pole	4.85 W
Mechanical service life (switching cycles) / typical	15 000
Electrical endurance (switching cycles) / at AC-1 / at 380/415 V 50/60 Hz	8 000
Neutral conductors / upgradeable/retrofittable	No

Ground fault monitoring version	Without
Product function	
• communication function	No
• other measurement function	No
Net weight	0.687 kg

Electricity

Max. rated operational voltage of the size of the circuit-breaker	160 A
Courant permanent assigné Iu	50 A
Operating current	
• at 40 °C	50 A
• at 45 °C	50 A
• at 50 °C	50 A
• at 55 °C	49 A
• at 60 °C	48 A
• at 65 °C	46 A
• at 70 °C	45 A

Switching capacity according to IEC 60947

Switching capacity class of the circuit breaker	S
Maximum short-circuit current breaking capacity (Icu)	
• at 240 V	55 kA
• at 415 V	36 kA
Operational short-circuit current breaking capacity (Ics)	
• at 240 V	55 kA
• at 415 V	36 kA
Short-circuit current making capacity (Icm)	
• at 240 V	121 kA
• at 415 V	76 kA

Adjustable parameters

Adjustable response value current / I _g min.	50 A
Adjustable response value current / I _g min.	50 A
Short-term delayed / tripping switchable / I _{2t} =ON/OFF	No
Adjustable response value current / I _i min.	500 A
Adjustable response value current / I _i max.	500 A
Ground fault protection / tripping switchable / I _{2t} =ON/OFF	No

Mechanical Design

Height [in]	5.1 in
Height	130 mm

Width [in]	2 in
Width	50.8 mm
Depth [in]	2.8 in
Depth	70 mm

Connections

Arrangement of electrical connectors / for main current circuit	Front terminal
Type of electrical connection / for main current circuit	box terminal
Type of connectable conductor cross-section, round conductor terminal, stranded	1 x (1.5 - 70 mm²)

Auxiliary circuit

Number of CO contacts / for auxiliary contacts	0
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Accessories

Product extension / optional / motor drive	No
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Environmental conditions

Protection class IP / on the front	IP40
Ambient temperature	
• during operation / minimum	-25 °C
• during operation / maximum	70 °C
• during storage / minimum	-40 °C
• during storage / maximum	80 °C

Certificates

Equipment marking / acc. to DIN EN 81346-2	Q
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General Product Approval	EMC	Declaration of Conformity
 CCC	 EAC	 EG-Konf.
 VDE	 RCM	

[KC](#)

Test Certificates	other
Type Test Certificates/Test Report	Miscellaneous
Special Test Certificate	Miscellaneous

Further information

Information- and Downloadcenter (Catalogs, Brochures,...)

<http://www.siemens.com/lowvoltage/catalogs>

Industry Mall (Online ordering system)

<https://mall.industry.siemens.com/mall/en/en/Catalog/product?mlfb=3VA1150-4ED26-0AA0>

Service&Support (Manuals, Certificates, Characteristics, FAQs,...)

<https://support.industry.siemens.com/cs/ww/en/ps/3VA1150-4ED26-0AA0>

Image database (product images, 2D dimension drawings, 3D models, device circuit diagrams, ...)

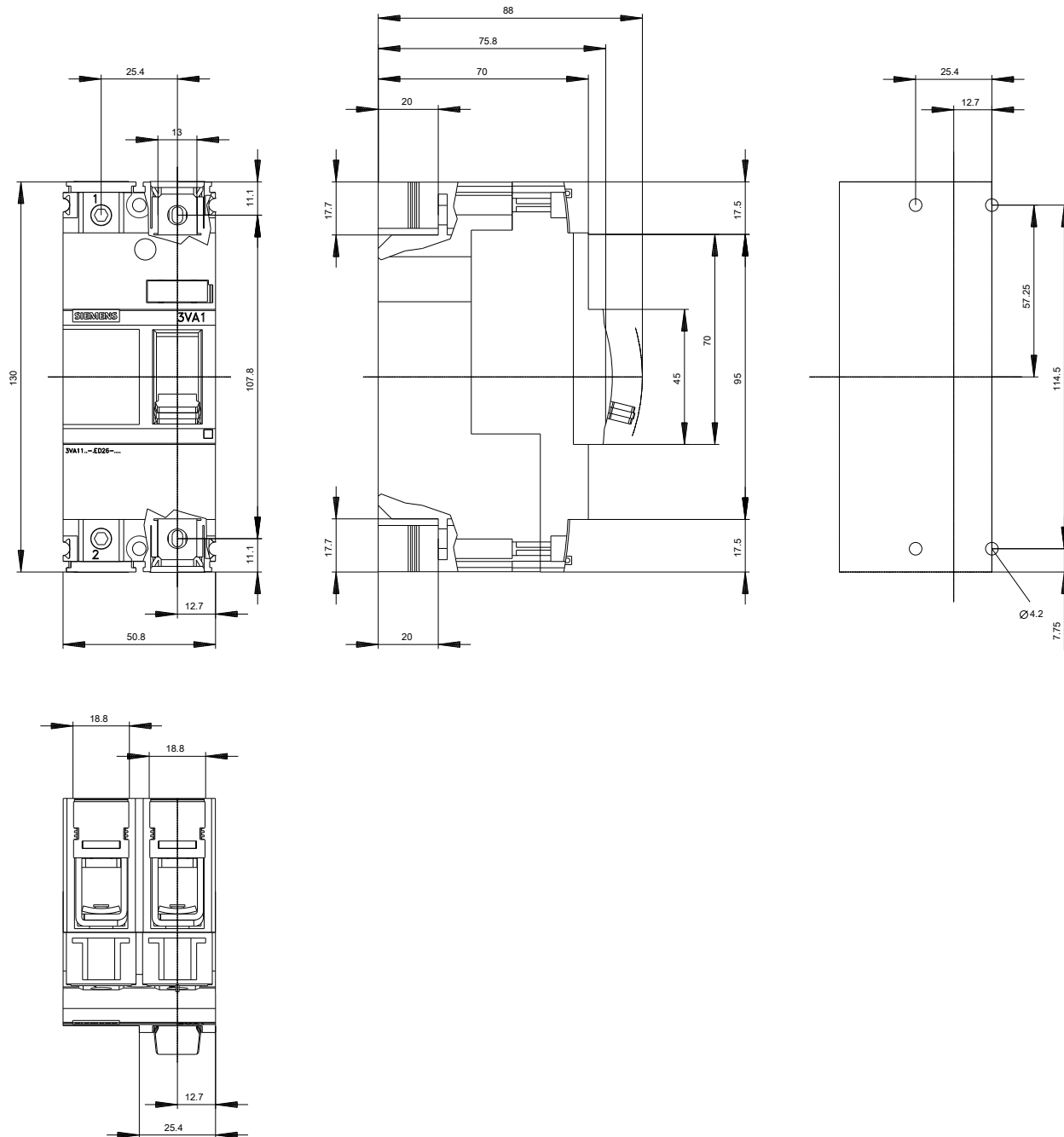
http://www.automation.siemens.com/bilddb/cax_en.aspx?mlfb=3VA1150-4ED26-0AA0

CAX-Online-Generator

<http://www.siemens.com/cax>

Tender specifications

<http://www.siemens.com/specifications>



The diagram illustrates a quantum circuit for a 2-qubit system. The circuit is composed of two parallel stages. Each stage involves a control qubit (top) and a target qubit (bottom). The control qubit is initialized to $|0\rangle$ and the target qubit to $|1\rangle$. In the first stage, the control qubit is controlled by a CNOT gate on the target qubit. In the second stage, the target qubit is controlled by a CNOT gate on the control qubit. The final state is $|00\rangle$.

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